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1 A spatial path scheduling algorithm for EDGE architectures

Katherine E. Coons, Xia Chen, Doug Burger, Kathryn S. McKinley, Sundeep K. Kushwa

November 2006 **ASPLOS-XII:** Proceedings of the 12th international conference on Arc for programming languages and operating systems

Publisher: ACM Request Permissions

Full text available: Pdf (651.48 KB) Additional Information: full citation, abstract, references, cit

Bibliometrics: Downloads (6 Weeks): 12, Downloads (12 Months): 92, Citation Count: 9

Growing on-chip wire delays are motivating architectural features that expose on-c to the compiler. EDGE architectures are one example of communication-exposed m which the compiler forms dataflow graphs that specify ...

Keywords: EDGE architecture, instruction scheduling, path scheduling, simulated

Also published in:

October 2006 **SIGOPS Operating Systems Review** Volume 40 Issue 5

October 2006 **SIGARCH Computer Architecture News** Volume 34 Issue 5

November 2006 **SIGPLAN Notices** Volume 41 Issue 11

2 Optimal versus Heuristic Global Code Scheduling

Sebastian Winkel

December 2007 **MICRO '07:** Proceedings of the 40th Annual IEEE/ACM International S Microarchitecture

Publisher: IEEE Computer Society

Full text available: Pdf (425.44 KB) Additional Information: full citation, abstract, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 78, Citation Count: 1

We present a global instruction scheduler based on inte- ger linear programming (I implemented exper- imentally in the Intel Itanium® product compiler. It features v scale of known EPIC scheduling optimiza- tions, more than ...

3 A Criticality Analysis of Clustering in Superscalar Processors

Pierre Salverda, Craig Zilles

November 2005 **MICRO 38:** Proceedings of the 38th annual IEEE/ACM International S Microarchitecture

Publisher: IEEE Computer Society

Full text available: Publisher Site, Pdf (448.82 KB) Additional Information: full citation, abstract, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 25, Citation Count: 4

Clustered machines partition hardware resources to circumvent the cycle time pena

large, monolithic structures. This partitioning introduces a long inter-cluster forwar potential for load imbalance, both of which ...

4 Matrix scheduler reloaded

Peter G. Sassone, Jeff Rupley, II, Edward Brekelbaum, Gabriel H. Loh, Bryan Black

June 2007 **ISCA '07:** Proceedings of the 34th annual international symposium on Co

Publisher: ACM

Full text available: Pdf (340.97 KB) Additional Information: full citation, abstract, references, inc

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 66, Citation Count: 2

From multiprocessor scale-up to cache sizes to the number of reorder-buffer entrie wish to reap the benefits of more computing resources while staying within power a This tension is quite evident in schedulers, which ...

Keywords: matrix, microarchitecture, picker, scheduler, wakeup

Also published in:

June 2007 **SIGARCH Computer Architecture News** Volume 35 Issue 2

5 Dynamic Strands: Collapsing Speculative Dependence Chains for Reducing P Communication

Peter G. Sassone, D. Scott Wills

December 2004 **MICRO 37:** Proceedings of the 37th annual IEEE/ACM International S Microarchitecture

Publisher: IEEE Computer Society

Full text available: Pdf (350.47 KB) Additional Information: full citation, abstract, references, cit

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 15, Citation Count: 12

In the modern era of wire-dominated architectures, specific effort must be made to communication within out-of-order pipelines while still maintaining binary compatib pressure on highly-connected elements such as the issue ...

6 FLASH: Foresighted Latency-Aware Scheduling Heuristic for Processors with Datapaths

Manjunath Kudlur, Kevin Fan, Michael Chu, Rajiv Ravindran, Nathan Clark, Scott Mah

March 2004 **CGO '04:** Proceedings of the international symposium on Code generatior feedback-directed and runtime optimization

Publisher: IEEE Computer Society

Full text available: Pdf (395.78 KB) Additional Information: full citation, abstract, references, inc

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 23, Citation Count: 1

Application-specific instruction set processors (ASIPs) have the potential to meet th performance,and power goals of future embedded processors bycustomizing the ha application. A centralproblem is creating compilers ...

7 Application-Specific Processing on a General-Purpose Core via Transparent Ir Customization

Nathan Clark, Manjunath Kudlur, Hyunchul Park, Scott Mahlke, Krisztian Flautner

December 2004 **MICRO 37:** Proceedings of the 37th annual IEEE/ACM International S Microarchitecture

Publisher: IEEE Computer Society

Full text available: Pdf (302.95 KB) Additional Information: full citation, abstract, references, cit

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 30, Citation Count: 18

Application-specific instruction set extensions are an effective way of improving the processors. Critical computation subgraphs can be accelerated by collapsing them i that are executed on specialized function units. ...

8 Design and Evaluation of Hybrid Fault-Detection Systems

George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, David I. August, St Mukherjee

June 2005 **ISCA '05:** Proceedings of the 32nd annual international symposium on Cc

Publisher: ACM

Full text available: Pdf (177.47 KB) Additional Information: full citation, abstract, references, cit

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 64, Citation Count: 11

As chip densities and clock rates increase, processors are becoming more susceptib faults that can affect program correctness. Up to now, system designers have prim hardware-only and software-only fault-detection mechanisms ...

Also published in:

May 2005 **SIGARCH Computer Architecture News** Volume 33 Issue 2

9 Predictable execution adaptivity through embedding dynamic reconfigurability schedules

Chengmo Yang, Alex Orailoglu

September 2007 **CODES+ ISSS '07:** Proceedings of the 5th IEEE/ACM international co Hardware/software codesign and system synthesis

Publisher: ACM

Full text available: Pdf (218.57 KB) Additional Information: full citation, abstract, references, inc

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 47, Citation Count: 0

Advances in semiconductor technologies have placed MPSoCs center stage as a sta for embedded applications of ever increasing complexity. Because of real-time cons are usually statically parallelized and scheduled ...

Keywords: adaptive execution, multiprocessor task schedulihng, reconfiguration

10 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **Transactions on Design Automation of Electronic Systems (TODA**

Publisher: ACM Request Permissions

Full text available: Pdf (550.02 KB) Additional Information: full citation, abstract, references, cit

Bibliometrics: Downloads (6 Weeks): 59, Downloads (12 Months): 401, Citation Count: 8

Low power has emerged as a principal theme in today's electronics industry. The n has caused a major paradigm shift in which power dissipation is as important as pe area. This article presents an in-depth survey of CAD methodologies ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dyna dissipation, energy-delay product, gated clocks, layout, low power layout, low powe power design, power analysis and estimation, power management, power minimiza management, probabilistic analysis, silicon-on-insulator technology, statistical sam capacitance, switching activity, symbolic simulation, synthesis, system design

11 Unified methodology for resolving power-performance tradeoffs at the microarc circuit levels

Victor Zyuban, Philip Strenski
August 2002 **ISLPED '02:** Proceedings of the 2002 international symposium on Low p
design
Publisher: ACM Request Permissions
Full text available: Pdf (127.01 KB) Additional Information: full citation, abstract, references, cit

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 41, Citation Count: 22

Evaluation of architectural tradeoffs is complicated by implications in the circuit dor
typically not captured in the analysis but substantially affect the results. We propos
hardware intensity (&eegr;), which is useful for ...

Keywords: energy, energy efficiency, hardware intensity, metric, power

12 Proceedings of the 2008 ACM symposium on Applied computing
Roger L. Wainwright, Hisham M. Haddad
March 2008 **SAC '08:** Proceedings of the 2008 ACM symposium on Applied computing
Publisher: ACM
Additional Information: full citation, abstract

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation Count: 0

Welcome to the 23rd Annual ACM Symposium on Applied Computing (SAC 2008). T
event is dedicated to computer scientists, engineers, and practitioners seeking innc
various areas of computer applications. This year, the conference ...

13 An Analysis of Efficient Multi-Core Global Power Management Policies: Maxim
for a Given Power Budget
Canturk Isci, Alper Buyuktosunoglu, Chen-Yong Cher, Pradip Bose, Margaret Martono
December 2006 **MICRO 39:** Proceedings of the 39th Annual IEEE/ACM International S
Microarchitecture
Publisher: IEEE Computer Society
Full text available: Pdf (523.46 KB) Additional Information: full citation, abstract, references, cit

Bibliometrics: Downloads (6 Weeks): 36, Downloads (12 Months): 241, Citation Count: 1

Chip-level power and thermal implications will continue to rule as one of the primar
and performance limiters. The gap between average and peak power actually wider
levels of core integration. As such, if per-core ...

14 Serialization-Aware Mini-Graphs: Performance with Fewer Resources
Anne Bracy, Amir Roth
December 2006 **MICRO 39:** Proceedings of the 39th Annual IEEE/ACM International S
Microarchitecture
Publisher: IEEE Computer Society
Full text available: Pdf (404.17 KB) Additional Information: full citation, abstract, references, inc

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 15, Citation Count: 2

Instruction aggregation-the grouping of multiple operations into a single processing
technique that has recently been used to amplify the bandwidth and capacity of cri
structures. This amplification can be used to improve IPC ...